What is Claimed is:

[c1] An integrated circuit, comprising:

a predefined block of functional circuitry having a plurality of I/O pins; and

a backside I/O pad electrically connected to each I/O pin through a backside via of the integrated circuit.

[c2] The integrated circuit of claim 1, wherein said I/O pins are formed in a lower interconnect level of an integrated circuit chip.

[c3] The integrated circuit of claim 1, wherein said I/O pins are formed in a lowest interconnect level of an integrated circuit chip.

[c4] The integrated circuit of claim 1, wherein said integrated circuit is fabricated using a bulk silicon substrate or using a silicon-on-insulator substrate.

[c5] The integrated circuit of claim 1, wherein said predefined block of functional circuitry includes a first portion containing functional circuitry and a second portion containing said I/O pins.

[c6] The integrated circuit of claim 5, wherein said backside vias connect to said I/O pins in said second portion.

[c7] The integrated circuit of claim 1, further including:

a plurality of frontside I/O pads; and

additional I/O pins, each additional I/O pin electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection.

[c8] The integrated circuit of claim 1, further including non-predefined circuitry.

[c9] The integrated circuit of claim 8, further including:

a plurality of frontside I/O pads; and

said non-predefined circuitry having a plurality of I/O pins, each I/O pin of said non-predefined circuitry electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection.

[c10] The integrated circuit of claim 9, further including:

additional predefined circuit I/O pins, each additional predefined circuit I/O pin electrically connected to one frontside I/O pad of the integrated circuit by a global wiring connection.

[c11] A method of making electrical connection to an integrated circuit, comprising:

providing a predefined block of functional circuitry having a plurality of I/O pins; and

connecting a backside I/O pad electrically to each I/O pin through a backside via of the integrated circuit.

[c12] The method of claim 11, further including:

providing additional I/O pins; and

electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection.

[c13] The method of claim 11, further including providing non-predefined circuitry.

[c14] The method of claim 13, further including:

providing a plurality of frontside I/O pads; and

electrically connecting one frontside I/O pad to a non-predefined circuit I/O pin by a global wiring connection.

[c15] The method of claim 14, further including:

providing additional predefined circuit I/O pins; and

electrically connecting each additional I/O pin to one frontside I/O pad of the integrated circuit by a global wiring connection.

[c16] The method of claim 11 further including:

forming said backside via in a bulk silicon substrate or a silicon on insulator substrate.

[c17]

An electronic device, comprising:

(a) an integrated circuit package;

(b) an integrated circuit chip comprising:

(i) a predefined block of functional circuitry having a plurality of first I/O pins, each first I/O pin electrically connected to a backside

I/O pad of the integrated circuit; and

(ii) non-predefined functional circuitry having a plurality of second I/O pins, each second I/O pin electrically connected to a frontside I/O pad of the integrated circuit;

(c) first connection means for electrically connecting each backside I/O pad to one pad of a first set of package pads of said integrated circuit package; and

(d) second connection means for electrically connecting each frontside I/O pad to one pad of a second set of package pads of said integrated circuit package.

[c18] The electronic device of claim 17, wherein said first connection means includes wirebonds, and wherein said second connection means includes solder balls.

[c19] The electronic device of claim 18, further including:

a second chip, said second chip having backside wirebond pads, each backside wirebond pad electrically connected to one pad of a third set of package pads of said integrated circuit package by a solder ball;

additional first I/O pins, each additional first I/O pin electrically connected to an additional backside I/O pad of the integrated circuit; and

wirebonds connecting each additional backside I/O pad to one backside wirebond pad of said second chip.

[c20] The electronic device of claim 17 wherein, said second connection means includes wirebonds to backside wirebond pads on a second chip, each backside wirebond pad on said second chip electrically connected to one frontside solder ball on said second chip, said frontside solder ball electrically connected to one pad of said second set of package pads of said integrated circuit package, and wherein, said second connection means includes solder balls.

[c21] An electronic device, comprising:

(a) a first integrated circuit chip comprising:

(i) a predefined block of functional circuitry having a plurality of first I/O pins, each first I/O pin electrically connected to a backside I/O pad of the integrated circuit; and

(ii) non-predefined functional circuitry having a plurality of second I/O pins, each second I/O pin electrically connected to a frontside I/O pad of the integrated circuit;

(b) a second integrated circuit chip mounted to a back surface of said first integrated circuit chip, said second integrated circuit chip having a plurality of frontside I/O pads; and

(c) connection means for electrically connecting each backside I/O pad of said first integrated circuit chip to one frontside I/O pad of said second integrated circuit chip.

[c22] The electronic device of claim 21, wherein said connection means is selected from the group consisting of C4 balls and wirebonds.